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DOCUMENT-IDENTIFIER: US 4430706 A

TITLE: Branch prediction apparatus and method for a data processing system

Detailed Description Paragraph Right (10):

In the preferred embodiment, prediction bits are stored in a read-write memory 21 which may simply be a read-write random access memory containing, for example, 4,096 bits wherein each bit is accessed in response to a respective hash-transformed microinstruction address derived from the address selector 18 via a multiplexer 26 and a conventional hashing circuit 24. As is well known, a hashing circuit serves to transform scattered input data (such as the microinstruction addresses provided by address selector 18 in FIG. 1) into a more compact and orderly form, such as is desirable for memory addressing. For example, hashing circuit 24 may simply extract a predetermined number of the least significant bits from the full microinstruction address, or, as another example, may simply reduce pairs of bits of the full microinstruction address into single bits using an "exclusive or" function. An example of a known type of hashing circuit is disclosed in U.S. Pat. No. 4,215,402 issued July 29, 1980, G. R. Mitchell and M. E. Houdek, inventors.